SEMESTER S7

VLSI ARCHITECTURES FOR DSP

Course Code	**PEEVT 757**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	VLSI	**Course Type**	Theory

Course Objectives:

1. Equip students with the ability to represent DSP algorithm Representations and Techniques
2. Develop student's proficiency in designing and implementing pipelined and parallel processing structures for DSP applications
3. Enable students to apply retiming and transformation techniques:
4. Train students to analyze and compute scaling and round-off noise in digital filters.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Representations of DSP algorithms - Block Diagram, Signal Flow Graph, Data Flow Graph, Dependence Graph. Loop Bound & Iteration Bound, Definition, Examples, Algorithms for Computing Iteration Bound – Longest Path Matrix Algorithm, Minimum Cycle Mean Algorithm, Iteration Bound of Multirate Data-Flow Graphs.	**9**
2	Pipelining and Parallel Processing - Pipelining of FIR Digital Filters, Data-Broadcast Structures, Fine-Grain Pipelining. Parallel Processing, Pipelining, and Parallel Processing for Low Power. Retiming: Definition and Properties, Solving System of Inequalities, Retiming Techniques- Cutset Retiming and Pipelining, Retiming for Clock Period Minimization, Retiming for Register Minimization	**9**

3	Unfolding: Properties of Unfolding, Critical Path, Unfolding and Retiming, Application of Unfolding, Sample Period Reduction, Parallel Processing. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.	**9**
4	Scaling and round off noise – scaling and round off noise, state variable description of digital filters, scaling and round off noise computation, round off noise in pipelined IIR filters, Round off noise omputation using state variable description, slow down, retiming and pipelining	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Represent DSP algorithms using block diagrams, signal flow graphs, data flow graphs, and dependence graphs, and analyze iteration bounds using relevant algorithms.	**K3**
CO2	Demonstrate the ability to design, implement, and optimize pipelined and parallel processing structures for DSP systems, including FIR digital filters and data broadcast structures, focusing on low-power solutions.	**K4**
CO3	Apply retiming techniques to minimize clock periods and registers and use unfolding and folding transformations to optimize DSP architectures.	**K6**
CO4	Become Proficient in evaluating and mitigating scaling and round-off noise in digital filters, particularly in pipelined IIR filters, using state variable descriptions and related computation techniques.	**K5**
CO5	Design efficient DSP architectures by integrating knowledge of algorithm representations, pipelining, parallel processing, retiming, and noise mitigation techniques.	**K6**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	**3**	**2**	**3**	**2**	**1**							
CO2	**3**	**3**	**3**	**2**	**2**	**1**						
CO3	**3**	**3**	**2**	**3**	**2**	**1**						
CO4	**2**	**3**	**2**	**3**	**1**	**1**						
CO5	**3**	**3**	**3**	**3**	**2**	**2**						

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	VLSI DSP Systems- Design and Implementation	Keshab K Parhi	John Wiley	1st Edn 1999.
2	Digital Signal processing for multimedia systems	Keshab K Parhi and Takao Nishitami	CRC press	2018
3	Digital Signal Processing with Field Programmable Gate Arrays	Uwe Meyer-Baese	Springer	4th Edn, 2014
4	VLSI Design Methodology Development	Thomas Dillinger	Prentice Hall	1st Edn 1998
5	Advanced Digital Signal Processing and Noise Reduction	Saeed V. Vaseghi	Wiley	4th Edn 2008

Reference Books				
Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Understanding digital signal processing	Richard G Lyons	Pearson Education India	3,1997
2	DSP Integrated Circuits	Lars Wanhammar	Academic Press	1st Edn 1999
3	Digital Filter Design	T. W. Parks and C. S. Burrus	Wiley-Interscience	1st Edn 1987
4	Architectures for Digital Signal Processing	Peter Pirsch	John Wiley & Sons	1st Edn 1998
5	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste and David Harris	Pearson	4th Edn 2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc20_ee44/preview
2	https://www.youtube.com/playlist?list=PLT1QAv48lhQKwFZ0TkqpJaUm2LeW9226z

SEMESTER 7

AI AND ML FOR VLSI CAD

Course Code	**PEEVT 758**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	Machine Learning	**Course Type**	Theory

Course Objectives:

1. To provide students with a comprehensive understanding of the applications of Artificial Intelligence and Machine Learning in VLSI CAD.
2. To introduce students to the concept of Compact Process Models (CPM) in lithographic patterning, enabling them to develop and train machine learning models for accurate representation and optimization of the lithographic process.
3. To equip students with the skills to apply machine learning algorithms for various aspects of physical design, mask synthesis, and physical verification in VLSI, focusing on enhancing efficiency, accuracy, and automation.
4. To train students in using machine learning techniques for yield estimation, reliability analysis, and testing in high-volume VLSI manufacturing, improving process optimization, and reliability prediction.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Introduction to AI and ML in VLSI CAD:** Overview of AI and ML applications in VLSI CAD, Unsupervised, Supervised, and Semisupervised Learning, Introduction to neural networks and decision trees **Introduction to VLSI Design Methodologies:** VLSI Design Cycle - Physical Design Cycle - Design Styles and comparison of different Design Styles, Fabrication of VLSI Circuits. **Machine Learning for Compact Lithographic Process Models:** Introduction, Lithographic Patterning Process, Representation of Lithographic Patterning Process – Mask, Imaging, Resist & Etch Transfer Function, Compact process model machine learning problem statement, CPM Task, CPM Training Experience, Performance metrics, Supervised	9

	learning of a CPM	
2	**Neural Network Compact Patterning Models:** Neural Network Mask Transfer Function, Neural Network Image Transfer Function, Neural Network Resist Transfer Function, Neural Network Etch Transfer Function **Machine Learning for Mask Synthesis** Introduction, Machine Learning guided OPC, MLP Construction, ML-EPC, EPC Algorithm **Machine Learning in Physical Verification** Introduction, Machine Learning in Physical Verification – layout feature extraction & encoding, models for hotspot detection.	**9**
3	**Machine Learning in Mask Synthesis and Physical Design**: Machine Learning in Mask Synthesis – mask synthesis flow, Machine Learning for sub-resolution assist features, Machine Learning for optical proximity correction. Machine Learning in Physical Design - for datapath placement, routability driven placement, clock optimization, lithography friendly routing **Machine Learning for Manufacturing**: Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications	**9**
4	**Machine Learning for Yield and Reliability:** High-volume manufacturing yield estimation – Histogram with random sampling, Histogram with GPST-PS, Kernel density estimation. Machine learning-based aging analysis. **Learning-Based VLSI Test and Verification:** VLSI Testing Process, Off-Chip Testing, On-Chip Testing, Combinational Circuit Testing, Sequential Circuit Testing, Advantages of VLSI Testing, Machine Learning's Advantages in VLSI Design, Ease in the Verification Process, Time-Saving, 3Ps (Power, Performance, Price), Electronic Design Automation, System-Level Design, Logic Synthesis and Physical Design, Test, Diagnosis, and Validation, Verification, Challenges	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Apply AI and ML concepts to VLSI CAD problems	**K3**
CO2	Develop and train machine learning models for lithographic process modeling	**K6**
CO3	Implement machine learning algorithms for physical design automation and verification	**K3**
CO4	Analyze machine learning-based solutions for yield estimation and reliability in VLSI manufacturing	**K4**
CO5	Evaluate the effectiveness of AI/ML techniques in VLSI testing and verification	**K5**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**1**									
CO2	**3**	**2**	**2**	**1**							**1**	
CO3	**3**	**2**	**1**	**1**							**1**	
CO4	**3**	**2**	**1**	**2**								**1**
CO5	**3**	**2**	**1**	**2**								**1**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Joobbani, R. An Artificial Intelligence Approach to VLSI Routing.	Joobbani, R.	Springer Science & Business Media	2012
2	VLSI Physical Design Automation.	Sait, Sadiq.	World Scientific,	1999
3	Machine Learning in VLSI Computer-Aided Design.	Elfadel, Ibrahim.	Springer,	2019
4	VLSI Physical Design: From Graph Partitioning to Timing Closure.	Kahng, Andrew.	Springer Nature	2022
5	Machine Learning Applications in Electronic Design Automation.	Ren, Haoxing.	Springer Nature	2023

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Layout Optimization in VLSI Design.	Lu, Bing.	Springer Science & Business Media	2001
2	Machine Learning for VLSI Chip Design	Abhishek Kumar, Suman Lata Tripathi and K Srinivasa Rao	John Wiley & Sons	2023